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(54) Burn-in compensation for plasma display panels

(57) The burn-in effect is a serious problem for plasma display-panels (1). It can lead to a significant lifetime reduction of the panels. Therefore, a digital map for cell usage is created and can be used for active burn-in compensation of the long-term-burn-in problem. The implementation requires a burn-in memory (9).

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Description

[0001] The present invention relates to a device and method for compensating burn-in effects on display devices containing a plurality of luminous cells. Particularly the present invention relates to a burn-in compensation for Plasma Display Panels.

Background

[0002] A Plasma Display Panel (PDP) utilizes a matrix array of discharge cells which can only be "ON" or "OFF". Also unlike a CRT or LCD in which gray levels are expressed by analog control of the light emission, a PDP controls the gray level by modulating the number of light pulses per frame (sustain pulses). This time-modulation will be integrated by the eye over a period corresponding to the eye time response. For a better understanding, it will be reminded that to perform a grey scale rendition, a PDP is commonly divided in sub-lighting periods called sub-fields, each one corresponding to a bit of the input video picture data. For clarification, a sub-field is a period of time in which successively the following is being done with a cell.

1 - there is a writing/addressing period in which the cells is either brought to an excited state with a high voltage or left on its neutral state with lower voltage,
2 - there is a sustain period in which a gas discharge is made with short voltage pulses which lead to corresponding short lighting pulses. Only the cells previously excited will produce lighting pulses. There will not be a gas discharge in the cells in neutral state,
3 - there is an erasing period in which the charge of the cells are quenched.

[0003] In some specific plasma driving schemes, the addressing or erasing periods are not present in each sub-field. However, there is always a sustain period corresponding to the lighting of the panel.

[0004] More sustain discharges or pulses correspond to more peak luminance. More sustain discharges correspond also to a faster ageing of the corresponding cell phosphor. This phosphor ageing produces a loss in displayed luminance for the corresponding cell. If the same picture is displayed for a long time, the panel cells will not age at the same rate and a ghost picture (of the permanently displayed image) will be clearly perceptible to the human viewer (image sticking). In other words, the ghost image corresponds to the picture still visible as a shadow on every other scene, when this picture has been displayed a long time on a screen. For some panels that have displayed for an extremely long time the same picture, the ghost levels may become unacceptable, and the panel may have to be written off at a very early point in its lifetime. CRTs also suffer from same problem, but at a substantially lower degree.

[0005] In today's PDP manuals the user is strongly warned of the burn-in problem and of the pictures that might cause it. The user is at the same time warned that warranty will not cover burn-in damage. The reason for this is, that the PDP burn-in problem is one of the unsolved problems of PDP technology. The burn-in problem can be divided in a short-term burn-in and a long-term burn-in. On a PDP, two kinds of ghost images are existing :

In "Short term burning-in" : the ghost image (3 to 5 % of its original brightness) is mainly a positive image ("burned" cells are brighter than others) which will disappear after a short time (some minutes up to some hours). The origin is not completely clear yet but it seems that this effect is related to some kind of charges which have been accumulated during the time a cell stays ON. Later these charges improve the luminance emitted by the cell even if only priming is active in the frame period.
In "Long term burning-in" : the stable sticking image is a negative image ("burned" cells are darker than others) related to a kind of aging of the plasma cell. The cumulative amplitude can go up to 50% loss of luminance. The long term burning is the more critical issue since this effect is not reversible and could reach 50% luminance loss. All known ways of dealing with the long-term burn-in problem are preventive while this invention proposes a solution that can be considered corrective.

Invention

[0006] In view of that, it is the object of the present invention to provide a method and a device for compensating burn-in effects on display devices containing a plurality of luminous cells.

[0007] According to the present invention this object is solved by a method for compensating burn-in effects on display devices containing a plurality of luminous cells by recording an activity value of each or a group of said cells and controlling the gain of the signals for said cells on the basis of said recorded activity value.

[0008] Furthermore, the above mentioned object is solved by a device for compensating burn-in effects on display devices containing a plurality of luminous cells, said device being connectable to the signal path of said display device, including recording means for recording an activity value of each or a group of said cells and controlling means connected to said recording means for controlling the gain of the signals for said cells on the basis of said activity value.

[0009] Further favourable developments of the present invention are set out in the sub claims.

[0010] Thus, according to the present invention there may be created a digital map of the cell usage that can be used for active burn-in compensation of the long term-term burn-in problem. Consequently, there is sug-

gested a way of compensating burn-in effects which can be used to recover panels that have been misused, i.e. have displayed for a long time the same picture.

[0011] The digital map of cell usage requires large memory resources, which makes the present implementation of the idea expensive, but which will become more and more affordable in the near future, taking in consideration the dramatic constant price-erosion of memories.

Drawings

[0012] Exemplary embodiments of the invention are illustrated in the drawings and are explained in more detail in the following description. The drawings showing in

Figure 1 a diagram of panel efficiency;

Figure 2 the diagram of Figure 1 for defining the range of gain for which the correction is performed;

Figure 3 a block diagram of the signal processing for the burn-in compensation of the present invention.

Figure 4 sustain integration means in further detail;

Figure 5 the implementation of a burn-in gain control;

Figure 6 a burn-in multiplier in further detail; and

Figure 7 a hardware architecture for an active burn-in compensation.

Exemplary embodiments:

Active Burn-in Compensation Principle

Panel burn-in characteristic

[0013] On Figure 1 a diagram of panel efficiency is shown. This curve, to be denoted as panel burn-in characteristic, will be stored on a look-up table. This curve is a function of the panel technology. It shows a very strong drop of the panel efficacy, i.e. a very strong aging in a critical domain, at the beginning of the life time of the display panel. Subsequently, there is a slight aging in a medium domain and further on during the working time of the panel there is no serious aging in a stable domain.

[0014] The principle behind the active correction circuit will be to determine the actual operation point (H0, G0) as depicted in Figure 2. H0 is the number of panel equivalent operation hours (this number takes in consideration whether panel has displayed mostly dark or bright pictures). Once H0 is known, G0 is also known, being G0 the panel expected luminous gain, for a panel having H0 hours of operation.

[0015] Now the principle is as follows. For a damaged panel (the correction only makes sense for a damaged panel), the user will specify the range [Gmin Gmax] to which the correction is to take place, for example with the burn-in control signal BURNIN-CTL shown in Figure 3. This range might be for instance 10% around central value G0. This range will be set near to zero for very slightly damaged panels, and might be even higher than 10% for extremely burn-in damaged panels.

[0016] Compensation will be performed by a variable gain multiplier (burn-in gain). This means that cells that have been substantially more used than the average will be steered with gain 1.00 (to avoid exceeding digital range 0-255), cells that have had an average use will be steered with gain 0.90, and cells that have had minimum use will be steered with gain 0.80. The individual cell correction is possible because there is an accurate cell usage map, which can be translated in equivalent operation hours, and so an individual cell burn-in calculator can be evaluated.

[0017] The required correction level can be adjusted by the user, resorting to an internal test pattern (middle gray level). He has only to adjust the correction parameter so that this test pattern will no more suffer from ghost pictures.

Amount of SDRAM space required for the cell usage map

[0018] The cell usage map is obtained by accumulating all information relative to the lighting period of said cell.

[0019] Each cell will light approximately 1000 times per frame.

60 frames per second

3600 seconds per hour

100000 maximum hours of operation

$$1000*60*3600*100000=2.16 \times 10^{13}$$

48 bits are enough for 2.81×10^{14}

[0020] So if 48 bits are taken per cell:

W-VGA: 853*480*3 = 1 228 320 cells

W-XGA: 1365*768*3 = 3 144 960 cells

[0021] The number of required bits will be:

W-VGA: 58 959 360 (fits within a single 64 Mbit SDRAM)

W-XGA: 150 958 080 (fits within a single 256 Mbit SDRAM)

[0022] Following flash memory would be required:
64 Mbit flash for W-VGA
128 Mbit flash for W-XGA if the last six bits are not stored (rounding to a multiple of 64 sustain pulses seems to be quite acceptable)

Circuit Implementation

[0023] In this section there is described a possible circuit implementation for the dynamic burn-in compensation. The signal processing architecture will be described first, and in a short final section a possible hardware architecture will be described. On this presentation buses will be given a bitwidth which should be understood as a help for the presentation and which in an actual implementation may differ.

signal processing

[0024] On Figure 3 it is depicted how the burn-in compensation might be implemented:

[0025] The signal processing units for the compensation algorithm are integrated into a usual signal processing system for a plasma display panel 1. The video signals for red, green and blue colours, R, G, B are put into a video-degamma unit 2. In this example the input signals have a bit length of 8 bits, i.e. bit 0 to bit 7. The output signals are further processed under the control of a control circuit 6 by sub-field coding means 3, sent to frame memory 4 and converted in a serial/parallel converter 5 for driving the plasma display panel 1. The control circuit 6 is a Peak White Enhancement Controller 6, which obtains an average power AP for each picture from an average power measuring device 7 connected to the video-degamma means 2. The burn-in compensation means is connected between the video-degamma means 2 and the subfield coding means 3. As will be explained in more detail hereafter, the burn-in compensation means comprises a burn-in multiplier 11 connected at the output of the video degamma means 2, a burn-in gain control circuit 10, a burn-in memory 9 and a sustain integration circuit 8.

[0026] The compensation algorithm can be decomposed in two parts. The first part integrates the total number of sustain pulses that a cell has lighted during its life-time. The block sustain_integration 8 is a simple add accumulation block that essentially accumulates on external SDRAM memory 9 total life-time sustain pulses. In order to know the number of sustain pulses corresponding to a cell digital value, it is required to know the PWL[7:0] factor given by the Peak White Enhancement controller 6. This PWL[7:0] value will be high for dark pictures (low energy luminance content) and low for bright pictures (high energy luminance content).

[0027] The second part retrieves cell usage information from external SDRAM memory 9, and evaluates on block burn-in gain control 10 for every cell an estimation of equivalent hours that has been lit. It also evaluates an estimation for the panel average usage. Finally it generates three correction multiplying factors MR[9:0], MG [9:0] and MB [9:0], which is higher for cells with above average usage and lower for cells with below average usage. The multiplication burn-in correction is performed on block burn_in multiplier 11 by multiplying the signal levels R, G, B of the video-degamma means 2 with the multiplying factors MR, MG, MB. The R, G, B signals R(9:0), G(9:0), B(9:0) from the block 11 are sent to the sub-field coding circuit 3 for further processing taking in account the long burn-in problem.

sustain integration

[0028] On Figure 4 the sustain_integration block is further detailed. This block is essentially composed of 3 multipliers and 3 adders, being a standard multiply and accumulate stage.

[0029] The input signals of the burn-in multiplier 11 R, G, B having a bit length of ten bits are multiplied with a PWL factor from the PWE controller 6 by respective multipliers MULT. The output signals SR, SG, SB are added to the sustain values SRi, SGi, SBi of the burn-in memory 9 by adders ADD in order to obtain the output sustain signals SRo, SGo, SBo for the burn-in memory 9.

burn-in gain control

[0030] Block burn-in gain 10 might be implemented as depicted in Figure 5.

[0031] This block contains three hour estimators 12. It is actually a multiplier which multiplies the total number of displayed sustain pulses by a constant factor to obtain the equivalent hour usage. This factor is directly used for defining working hours when the experimental power burn-in characteristic was traced.

[0032] The block hour average 13 is used to obtain an average over all panel cells of the hour estimation values. The four thus obtained hour values HR[15:0], HG[15:0], HB [15:0] and H0 [15:0] are then transformed by the panel burn-in characteristic look-up table 14 in the corresponding estimated luminance efficacy (luminance gain): GR[9:0], GG[9:0], GB[9:0] and G0 [9:0].

[0033] The average panel gain G0 [9:0] is then mapped to a gain range where correction will be effective in block gain_range 15. This gain range 15, [Gmin Gmax], has to be directly controlled by the user function of panel damage, by means of parameter BURNIN_CTL [7:0]. It should be zero for instance if no burn-in markings are seen on the panel.

[0034] The block gain_limiter 16 limits the cell luminance gain factors to the just evaluated correction gain range.

[0035] Finally the gain_window block 17 maps the luminance gain factors to correction factors:

Gmin -> 1.00

GR -> 1.00 - (GR - Gmin)

GG -> 1.00 - (GG - Gmin)

GB -> 1.00 - (GB - Gmin)

Gmax-> 1.00 - (Gmax-Gmin)

burn-in multiplier

[0036] The burn-in multiplier 11 shown in Figure 6 is composed of the 3 multipliers that perform actual burn-in active correction. The output signals MR, MG, MB of the burn-in gain control 10 are multiplied by the input signals Ri, Gi, Bi form the video-degamma means 2 to obtain the output signals Ro, Go, Bo for the subfield coding means 3 and the sustain integration means 8.

hardware architecture

[0037] A practical implementation for active burn-in compensation might be realized according to Figure 7 (for W-VGA panels, but for other resolutions the same would apply with the corresponding memory sizes):

[0038] Most blocks will be probably integrated on the plasma controller ASIC 18. Located externally to the controller 18 there will be the memory Ics 9a, 9b, because such huge required Ics can not be easily integrated on the controller 8.

[0039] On the proposed solution (but it should be noted that other solutions are possible) there are two individual memory buses: Ds[31:0] for storing the 2 frames subfield information (subfield bus) and Db[31:0] for storing burn-in information (burn-in bus). New in this connection is the burn-in bus Db.

[0040] The operation principle is as follows: every time the panel 1 is powered-up, the controller 18 will quickly transfer all burn-in information stored on non-volatile FLASH memory 9a, to the external SDRAM 9b. During normal operation burn-in data will be read and written back from the SDRAM 9b, which allows for a very fast access and an almost unlimited number of writing operations. Finally when during power down data will be again transferred from the SDRAM 9b to the non-volatile FLASH 9a. For correct operation, and for the first time that panel is powered, then contents of the FLASH memory 9a should be obviously zero.

[0041] In an actual implementation some care will have to be taken that data is never lost. If the cell usage map is lost it can not be recovered, and burn-in active compensation possibilities are irreversibly lost for the panel in consideration. This is essentially a data security problem, for which there are known proven techniques, and which does not belong to the scope of this patent.

[0042] Thus, the present invention provides the following advantages:

- The long time burn-in artefact is digitally compensated in an active way.
- The recovery of panels that otherwise would have to be written-off is possible.
- The panel life time especially in professional applications, were the same kind of image is displayed for a long time (e.g. airports, libraries, train stations), is extended.

Claims

1. Method for compensating burn-in effects on a display device (1) containing a plurality of luminous cells by
   recording an activity value of each or a group of said cells and
   controlling the gain of the signals for said cells on the basis of said recorded activity value.

2. Method according to claim 1, wherein the display device (1) includes a Plasma Display Panel and the activity value is based on a frequency and/or a total number of sustain pulses having been used for driving said cells.

3. Method according to claim 1 or 2, wherein said recording includes storing said activity value in a memory (9).

4. Method according to claim 2 or 3, wherein a number of sustain pulses is calculated on the basis of peak white levels of pictures.

5. Method according to one of the claims 2 to 4, wherein said activity value includes a temporal value calculated on the basis of a number of sustain pulses.

6. Method according to one of the claims 1 to 5, wherein said controlling of the gain includes setting a gain on the basis of a look-up-table with said activity value as input signal.

7. Device for compensating burn-in effects on a display device (1) containing a plurality of luminous cells, said device being connectable to the signal path of said display device (1), including
   recording means (8, 9)for recording an activity value of each or a group of said cells and
   controlling means (10) connected to said recording means (8, 9) for controlling the gain of the signals for said cells on the basis of said activity value.

8. Device according to claim 7, wherein said display

device (1) includes a Plasma Display Panel and said recording means (8, 9) includes a sustain integration means (8) for calculating said activity value on the basis of a frequency and/or a total number of sustain pulses for driving said cells.

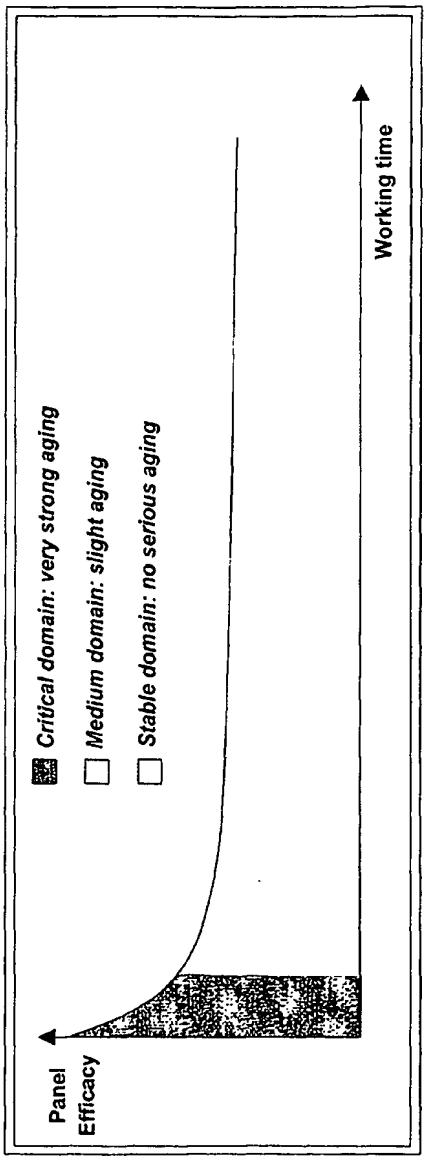
9. Device according to claim 7 or 8, wherein said recording means (8, 9) includes memory means (9) for storing said activity value.

10. Device according to claim 8 or 9, wherein said recording means (8, 9) includes peak white level determining means (6, 7) connected to said sustain integration means (8) for calculating a number of sustain pulses on the basis of peak white levels of pictures.

11. Device according to one of the claims 8 to 10, wherein said controlling means (10) includes hour estimation means 12) for calculating a temporal value on the basis of a number of sustain pulses as activity value.

12. Device according to one of the claims 7 to 11, wherein said controlling means (10) includes look-up-table means (14) for setting said gain on the basis of a look-up-table with said activity value as input signal.

FIG. 1


Critical domain: very strong aging
Medium domain: slight aging
Stable domain: no serious aging
Working time
Panel Efficacy

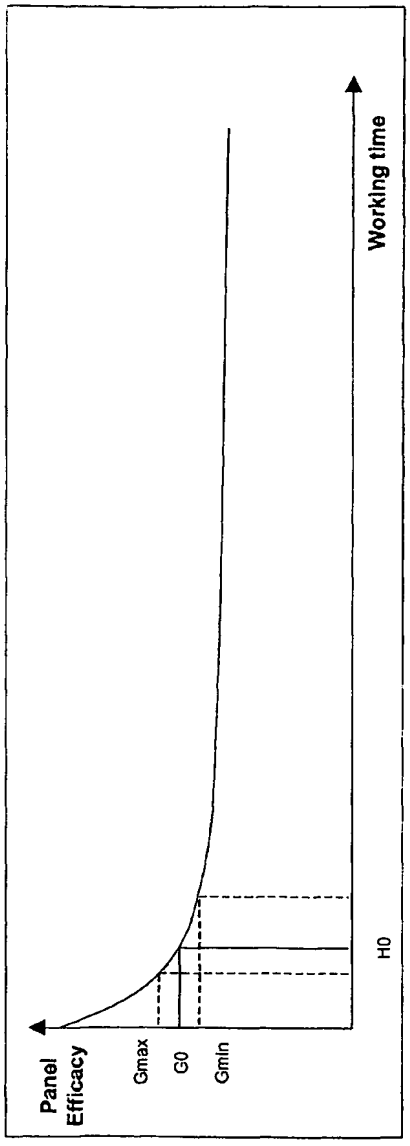

Working time
Panel Efficacy
Gmax
G0
Gmin
H0

FIG. 2

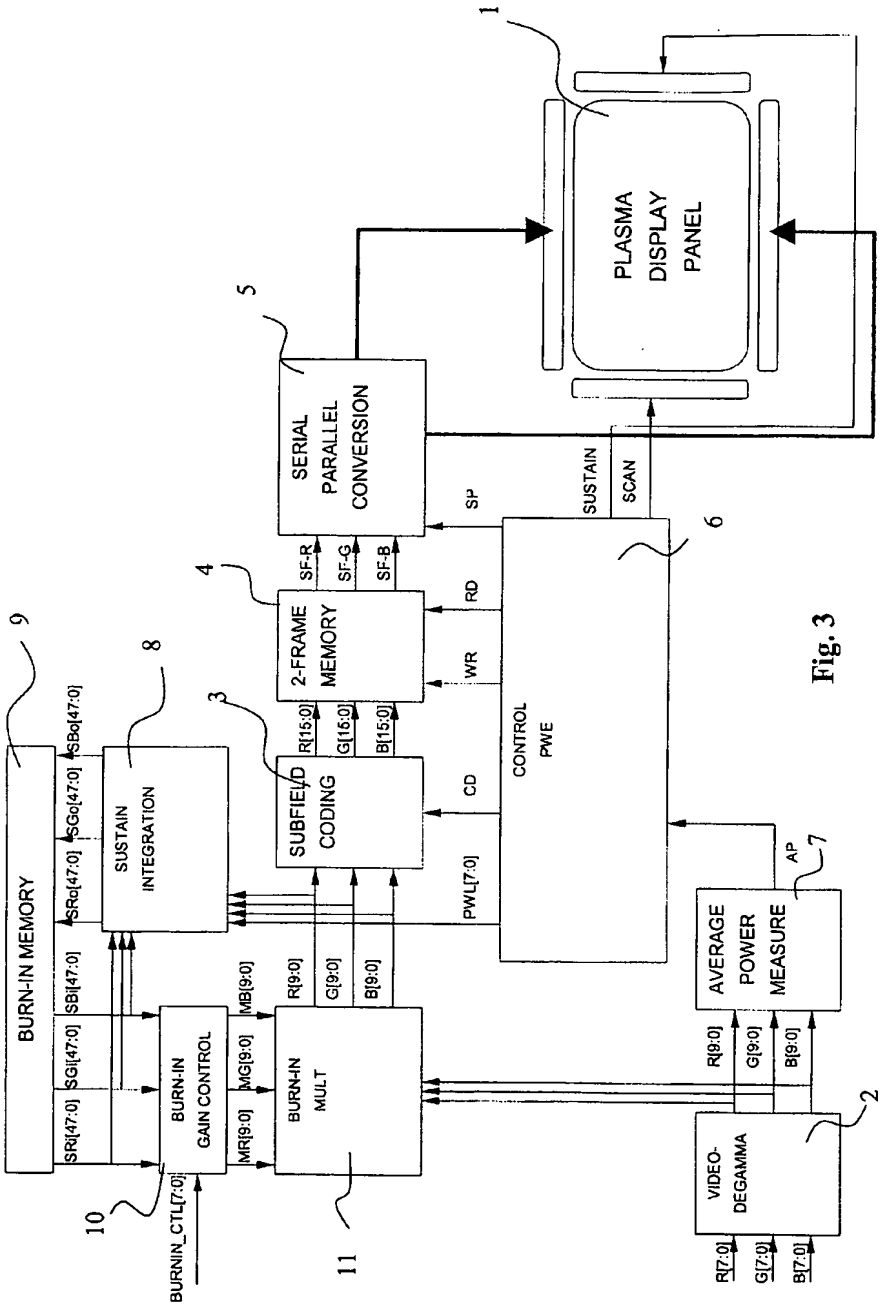
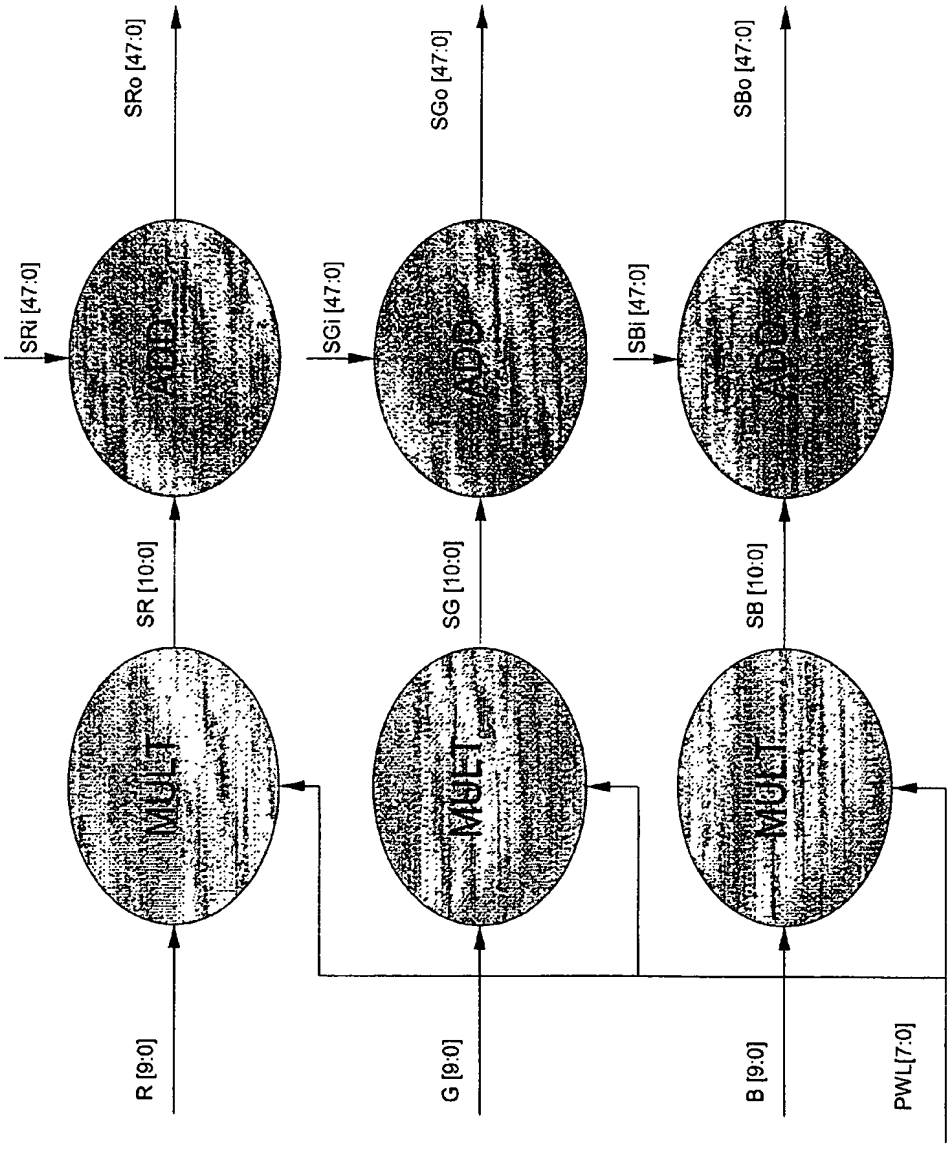

PLASMA DISPLAY PANEL
SERIAL PARALLEL CONVERSION
2-FRAME MEMORY
SUBFIELD CODING
CONTROL PWE
SUSTAIN INTEGRATION
BURN-IN MEMORY
BURN-IN GAIN CONTROL
BURN-IN MULT
AVERAGE POWER MEASURE
VIDEO-DEGAMMA
SF-R
SF-G
SF-B
SP
SUSTAIN
SCAN
RD
WR
CD
PWL[7:0]
AP
R[15:0]
G[16:0]
B[15:0]
SRo[47:0]
SGo[47:0]
SBo[47:0]
SRi[47:0]
SGi[47:0]
SBi[47:0]
MR[9:0]
MG[9:0]
MB[9:0]
R[9:0]
G[9:0]
B[9:0]
R[7:0]
G[7:0]
B[7:0]
BURNIN_CTL[7:0]
1
2
3
4
5
6
7
8
9
10
11

Fig. 3


R [9:0]
G [9:0]
B [9:0]
PWL[7:0]
MULT
MULT
MULT
SR [10:0]
SG [10:0]
SB [10:0]
ADD
ADD
ADD
SRi [47:0]
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SBi [47:0]
SRo [47:0]
SGo [47:0]
SBo [47:0]

Fig. 4

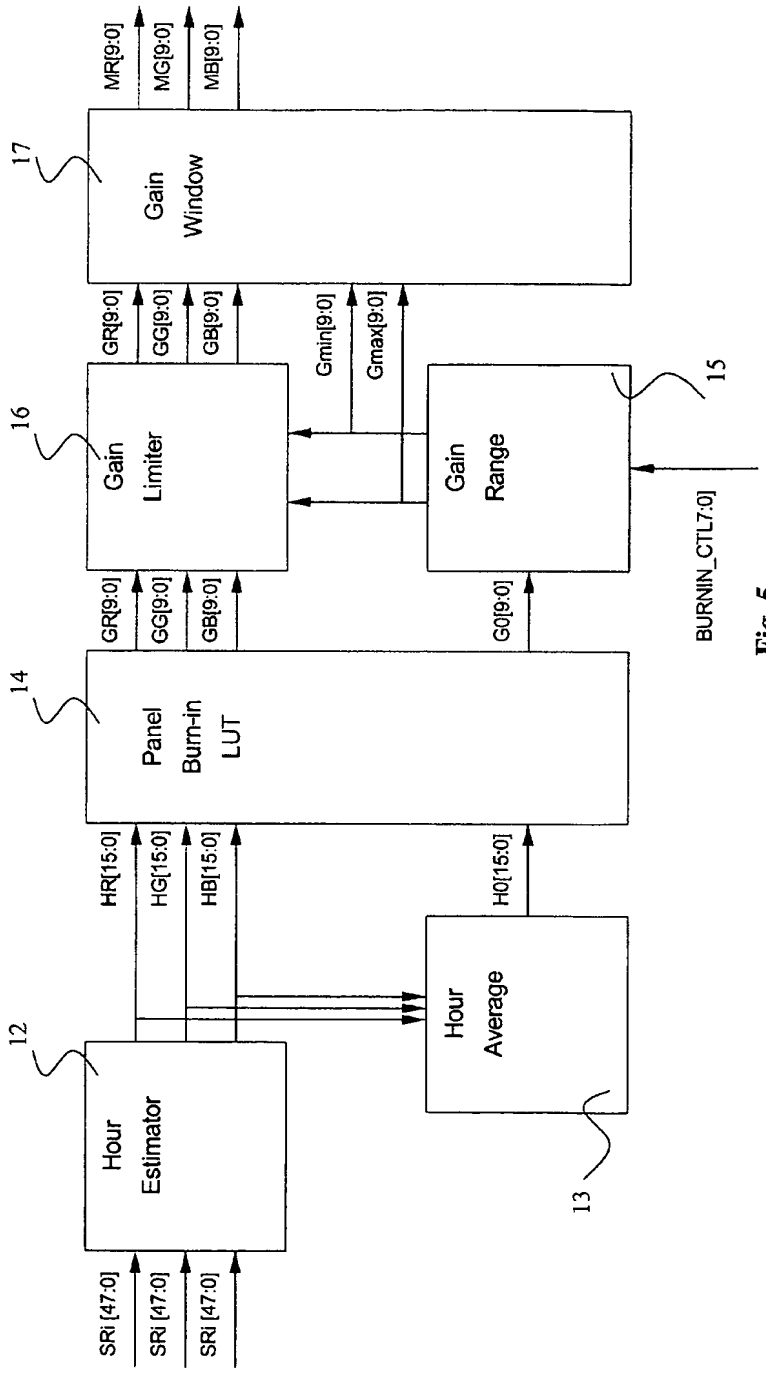
SRi [47:0]
SRi [47:0]
SRi [47:0]
12
Hour Estimator
HR[15:0]
HG[15:0]
HB[15:0]
Hour Average
H0[15:0]
13
14
Panel Burn-in LUT
GR[9:0]
GG[9:0]
GB[9:0]
G0[9:0]
16
Gain Limiter
Gain Range
15
BURNIN_CTL7:0]
Gmin[9:0]
Gmax[9:0]
GR[9:0]
GG[9:0]
GB[9:0]
17
Gain Window
MR[9:0]
MG[9:0]
MB[9:0]

Fig. 5

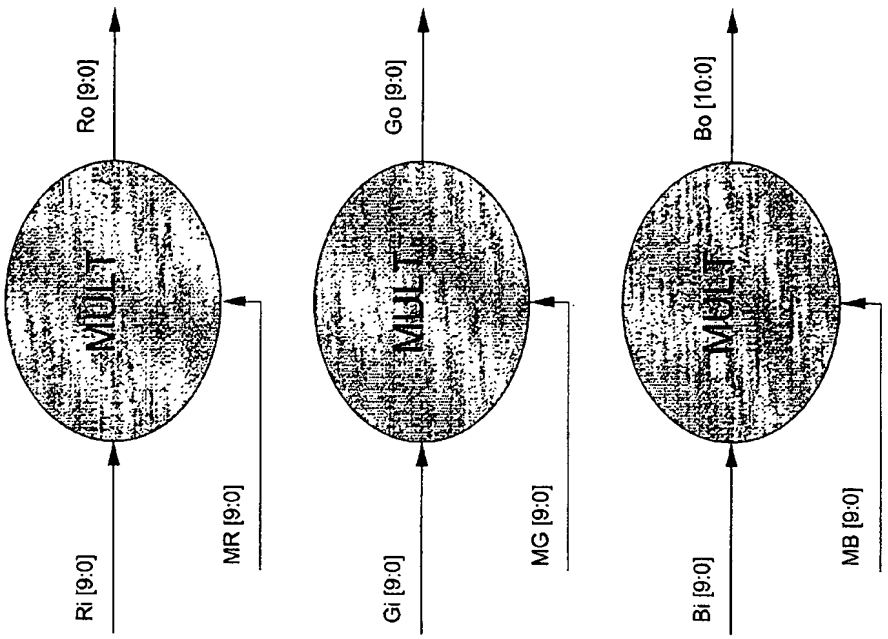

Fig. 6

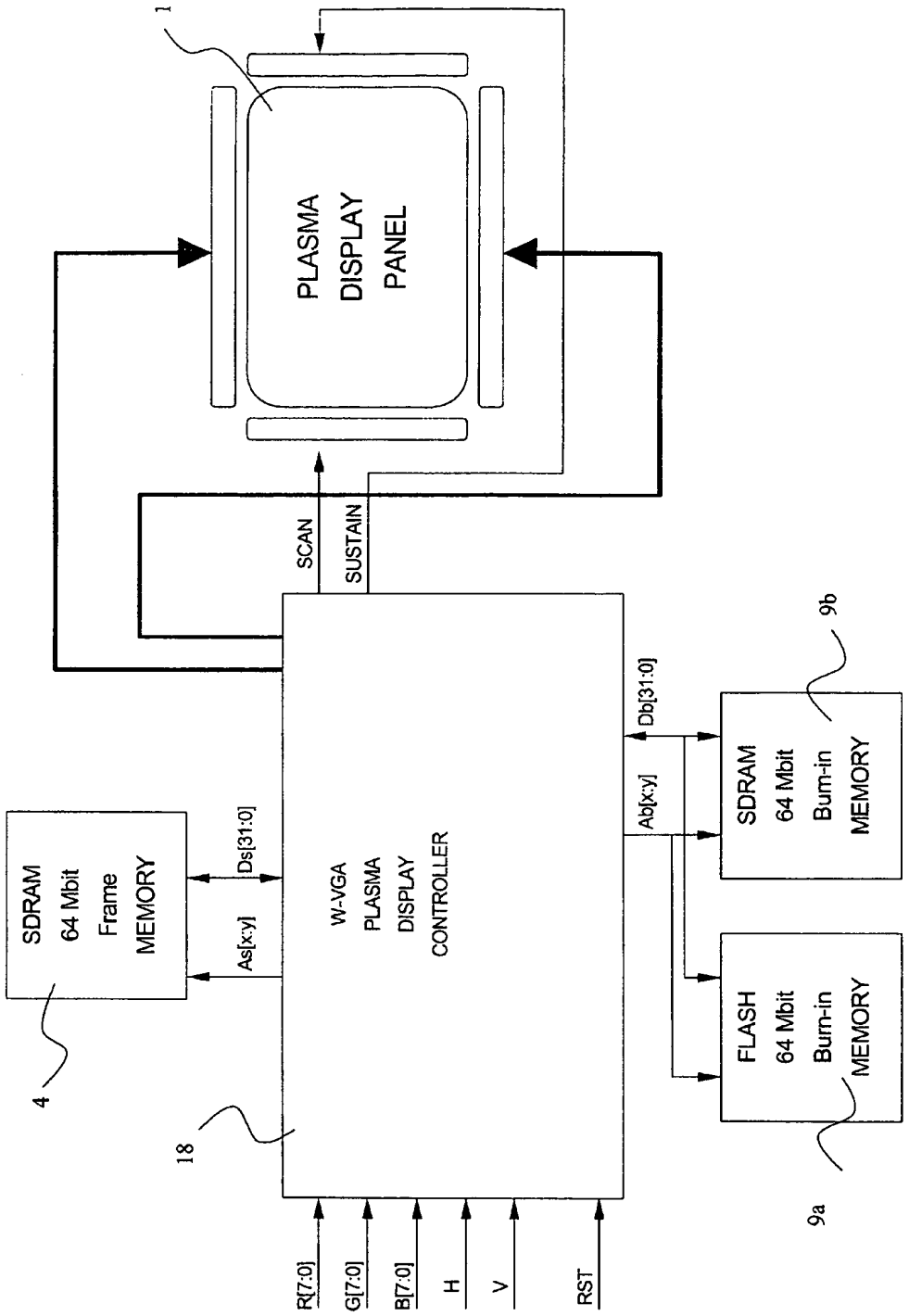
1
PLASMA
DISPLAY
PANEL
SCAN
SUSTAIN
SDRAM
64 Mbit
Frame
MEMORY
4
Ds[31:0]
As[x:y]
W-VGA
PLASMA
DISPLAY
CONTROLLER
18
Db[31:0]
Ab[x:y]
SDRAM
64 Mbit
Burn-in
MEMORY
9b
FLASH
64 Mbit
Burn-in
MEMORY
9a
R[7:0]
G[7:0]
B[7:0]
H
V
RST

Fig. 7

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EUROPEAN SEARCH REPORT

Application Number
EP 02 29 1489

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
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A	* abstract * * column 6, line 14 - line 35 * * column 8, line 16 - line 42 *	5,6,10, 11	
Y	US 5 493 183 A (KIMBALL ROBERT A) 20 February 1996 (1996-02-20)	1-4,7,9, 12	
A	* abstract * * column 2, line 38 - line 53; claim 1; figures 1-3 *	5,6,10, 11	
A	EP 1 047 040 A (NIPPON ELECTRIC CO) 25 October 2000 (2000-10-25) * abstract * * column 2, line 57 - column 3, line 35 * * column 7, line 23 - line 40; figure 2 *	1-12	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	27 November 2002	O'Reilly, D

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